CS 348B Project Report

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Introduction

In this project, we plan to render silicon wafers with the signature of rainbow colors on the reflecting surface. An array of IC's on a big silicon wafer is always favored for semiconductor manufacture to present their new chip products. The rainbow color on the metal and silicon dioxide patterns comes from diffraction and interference of the reflected light, which makes computer rendering challenging.

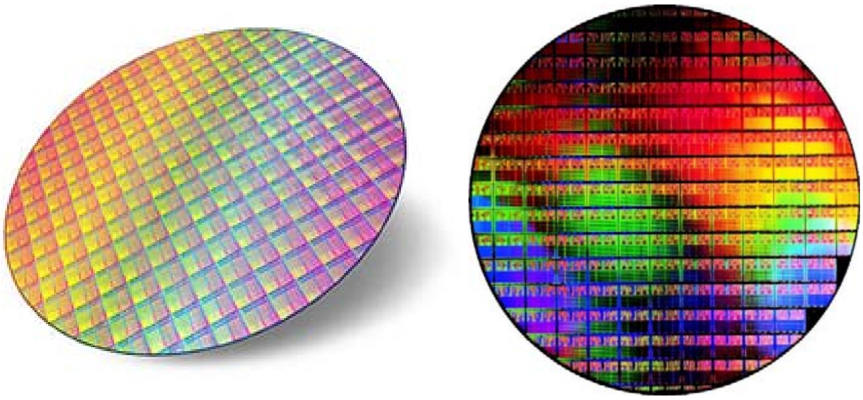
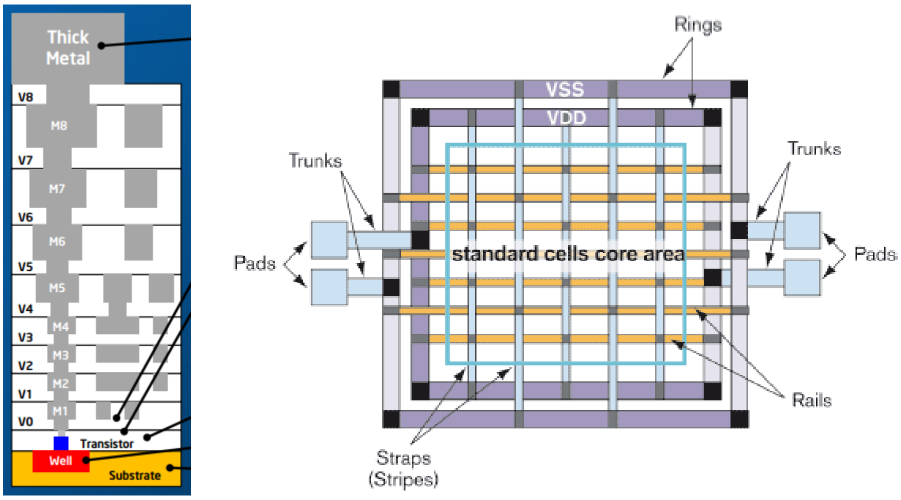


Figure 1. Silicon wafers with rainbow colors

Modeling

Since the goal for this project is to render silicon wafers from physical basis, we plan to model the wafer according to the real physical structure of semiconductor chips. In the most common CMOS technology, integrated circuits consist of a silicon substrate, which contains transistor devices, and layers of metal for wiring and interconnections. Top layers of metal are of thicker and wider geometrical size, and thus possess much lower resistance. Due to such features they are used extensively in power and ground distribution networks. Figure 2 (a) shows the structure of metal layers in Intel 32nm RF technology [1]. In this eight-metal-layer technology, for example, M7 and M8 are the top metal layers for power/ground networks. Figure 2 (b) shows the most commonly used power/ground mesh structure for the distribution networks. Note that in each metal layer, metal is routed either vertically or horizontally to avoid short circuit. In addition, vias are used for interconnection between layers. In this case, the light blue vertical straps most probably represent M8 layer metal in Intel 32nm RF technology, while the orange horizontal straps might be M7 layer metal.



(a) (b)

Figure 2. (a) metal layer structure of Intel 32nm RF technology. (b) Schematic of power and ground mesh network [2].

We have already known that metal is opaque and reflective while silicon dioxide filled in between is transparent. To further simplify the rendering model, we assume that most of the light we see from a wafer comes from reflection by silicon dioxide surface, the top metal layer and, of course, the interference among these reflected light, while that light that makes through the top metal is eventually absorbed by sub-surface structure. Figure 3 shows the simplified optical paths in the cross-section of wafer surface based on such assumption. Since the top metal for power/ground mesh has a very regular and repeating pattern, these reflected light rays have strong coherence.

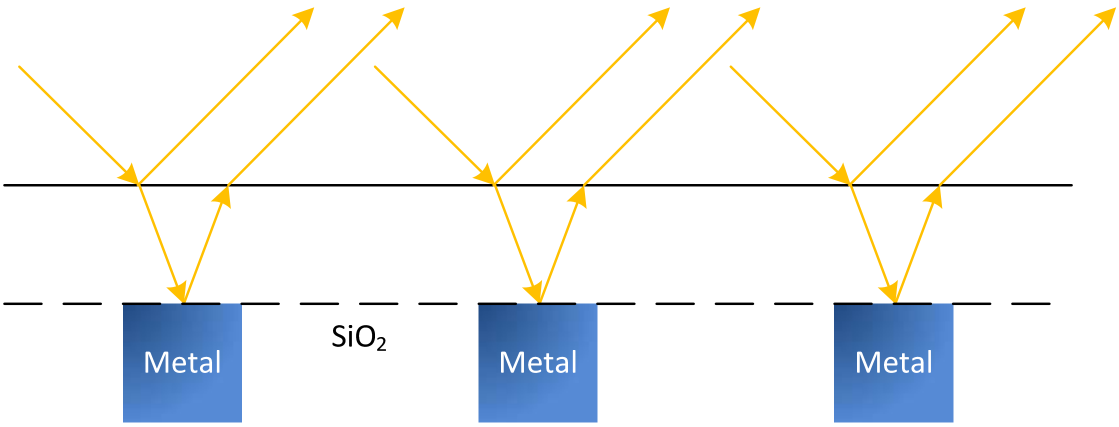


Figure 3. Simplified structure of the wafer surface

Another key aspect of modeling that we would like to address is the texture on a single chip. Figure 4 shows an image of Intel Westmere architecture. The colored texture in the chip does not represent the real color of the integrated circuits themselves but interference patterns instead. Based on chip design knowledge, we assume each set of blocks that has the exact same rainbow pattern (e.g. SRAM blocks with light blue boxes annotated) shares the same geometrical parameters (e.g. strap spacing) and optical parameters (e.g. reflection factor). On the other hand, blocks that have different parameters will have different rainbow patterns.

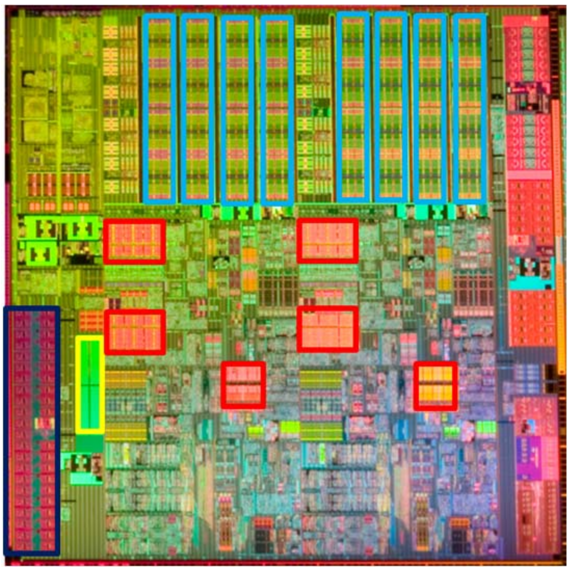


Figure 4. Intel Westmere architecture core with rainbow color

Physical Principles

The complicated structure of the wafer surface will result in various diffraction and interference effects, as shown in Figure 5. Previous study [3] only emphasized the interference between different wires. We well acknowledge the fact that comprehensive analysis of all such effects is necessary and essential, and discuss in detail the dominant effects followed by Bidirectional Reflectance Distribution Function (BRDF) accounting for all effects combined.

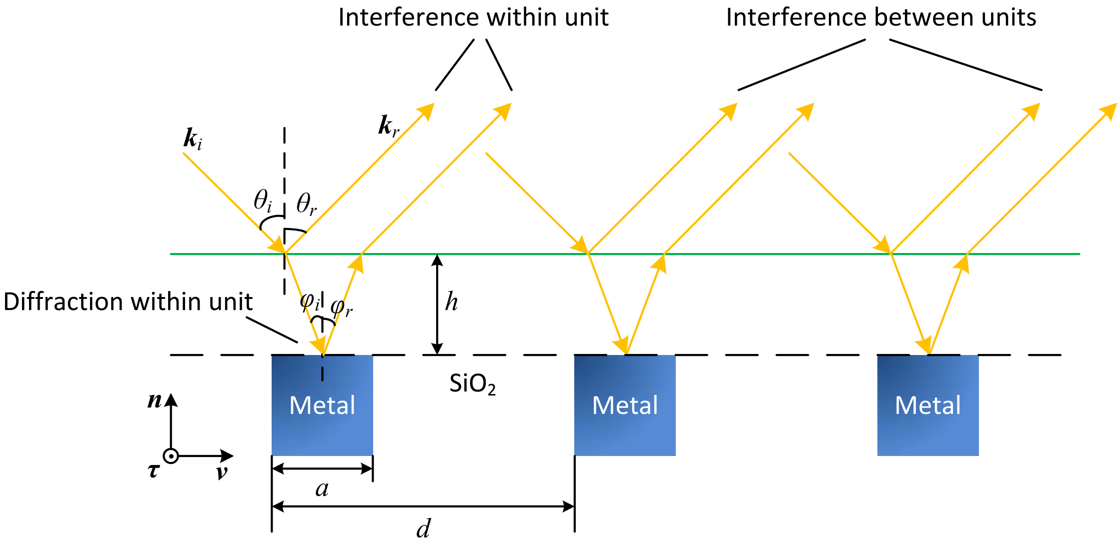


Figure 5. Various optical effects on wafer surface

Diffraction within Unit

First, when the light ray hits a tiny structure (here is the narrow metal wire), it will diffract. The reflected intensity factor depends on the optical path difference (OPD) of the rays at the two edges of the wire, which can be calculated from the width of the wire, a, and the incident and reflected angles, as

$$f_{DW} = \left(\frac{\sin\alpha}{\alpha}\right)^2, \quad \alpha = \frac{\pi}{\lambda} a(\sin\varphi_r - \sin\varphi_i)$$

Interference between Units

Another effect comes from the interference between the light rays reflected from different wires. The OPD depends on the distance between wires, i.e., the wire space d, and the directions of the incident and reflected rays.

$$f_{IB} = \left(\frac{\sin N\beta}{\sin\beta}\right)^2 \xrightarrow{N\to\infty} \sum_{k=-\infty}^{\infty} \delta(\beta - k\pi), \quad \beta = \frac{\pi}{\lambda} d\big((\boldsymbol{k}_r - \boldsymbol{k}_i)\cdot\boldsymbol{v}\big)$$

We can see that when the number of parallel wires N goes up to infinity, the factor approaches a sequence of delta functions, which means very sharp peaks.

Interference within Unit

Within a unit, there is also interference, which is between the light rays reflected from the top surface and from the metal wires. This is similar to thin film interference, and the factor is a cosine function of the OPD.

$$f_{IW} = (\cos\gamma)^2, \quad \gamma = \frac{\pi}{\lambda} nh\left(\cos\varphi_r + \frac{1 - \sin\varphi_r \sin\varphi_i}{\cos\varphi_i}\right)$$

Anisotropy

We can imagine when viewing along the parallel wires and perpendicular to the wires, we will see different reflected phenomena. So the anisotropic property of the surface needs to be taken into account, which gives a coefficient

$$c_a = \big((\boldsymbol{k}_r - \boldsymbol{k}_i)\cdot\boldsymbol{\tau}\big)^p$$

Non-diffraction Effects

At last we should add the basic optical properties of the surface when there is no diffraction or interference. Since they are not the main effects, we simply use diffuse reflection and specular reflection to model them.

To Put It All Together

The final BRDF, including all the effects above, are given by

$$f_r = f_{dr} + f_{sr} + c_a f_{IW} f_{IB} f_{DW}$$

Implementation

Based on the physics discussed in the previous section, we implement our ray tracer with interference and diffraction effects.

First we summarize all the parameters of the surface in Table 1. The values of the parameters are generated from some real circuits that use the up-to-date CMOS technology.

Table 1. Parameter list of wafer surface

Parameter	Description	Value
D	Spacing between wires	900 – 1300 nm
H	Thickness of top SiO_2 layer	530 nm
A	Width of wire	250 nm
Deg	Direction of the wire on surface	0°, 90°
N	Refractive index	1.544
R	Diffraction reflectivity	0.3 – 0.7
Ks	Specular reflectivity	0.3
Kd	Diffuse reflectivity	0

A key element is the delta function in f_{IB}. It is not practical to implement exact delta function with infinite amplitude and infinitesimal width, let alone the fact that there exists no delta function in reality, and that noise will make it expand to finite amplitude and width. Instead, we use Gaussian function as an alternative to approximate it. We tune the width of the Gaussian function for better appearance.

When calculating the BRDF of the wafer surface, the equations only present the relation between intensity and the wavelength explicitly. This can only be represented as sampled spectrum. However, usually RGB spectrum is simpler, also takes smaller memory space and has higher performance. So, we convert the sampled spectrum to RGB spectrum after getting the BRDF, and then use RBG in the rest of the ray tracing process.

Results

To examine each of the effects, we render example images, each of which has only one of the effects turned on.

First we find that the interference between units provides the main color strips, as shown in Figure 6. The left one is lit by a single light source, and contains clearly distinguished color strips. The right one is with multiple light sources, thus resulting in more complex color patterns.

Then Figure 7 shows the effect of interference within unit. As we said, this is just thin film interference. In different areas, due to the difference of the incident and reflected directions, different colors are enhanced, and we can see a soft color transition. This effect will modulate the color strips shown in Figure 6.

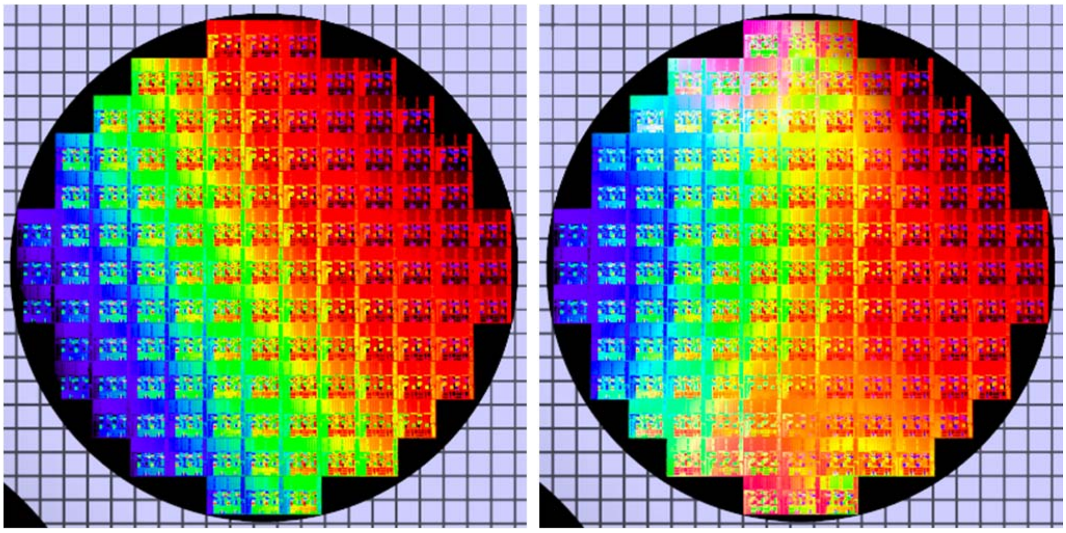


Figure 6. Images with interference between units only
(left: single point light source; right: multiple light source)

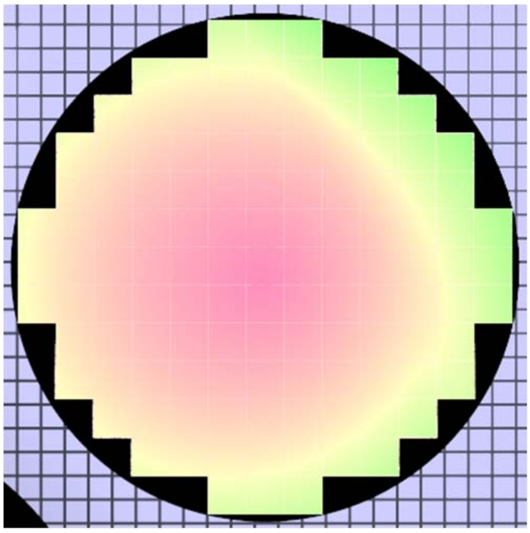


Figure 7. Images with interference within unit only

At last, we find that the diffraction within unit has no obvious contribution. That is because the width of the wire a, which determines the diffraction, is too small compared to the wavelength to generate obvious diffraction patterns.

Final Rendering

Putting all the elements together, we proudly present our final rendering image in Figure 8, the rendered pattern with one point light source and one spot light source. Surface parameters are generated from Table 1.

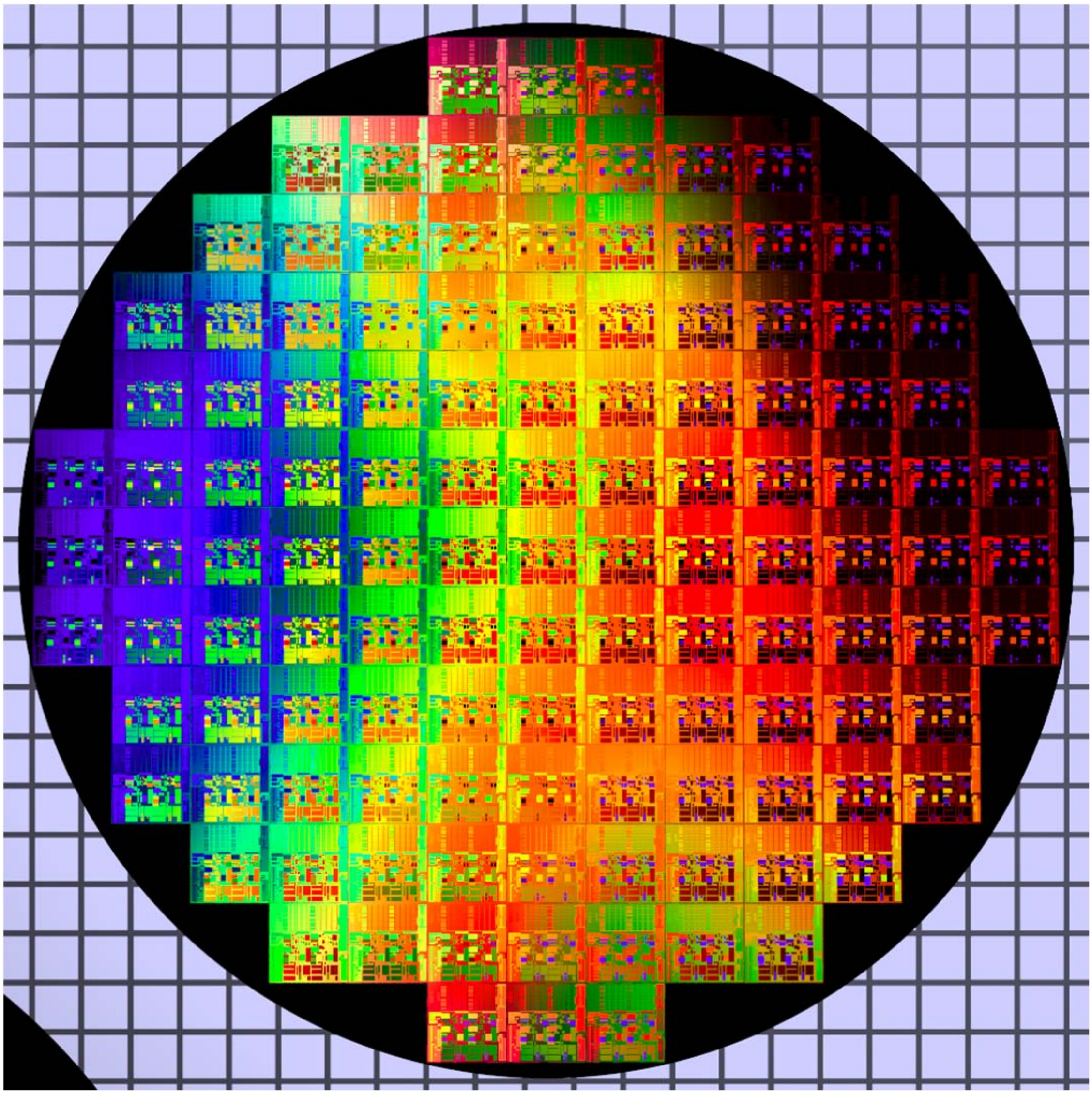


Figure 8. Final rendering

Comparing to the original image, (as shown in Figure 9), while the difference in the color distribution is discernable, many aspects of the appearance, including the color saturation, transition pattern, reflectivity, etc., are very similar between these two images. We believe the complex color distribution of the real photography is due to the complex light source system it uses. If we add more light sources, they will look more similar.

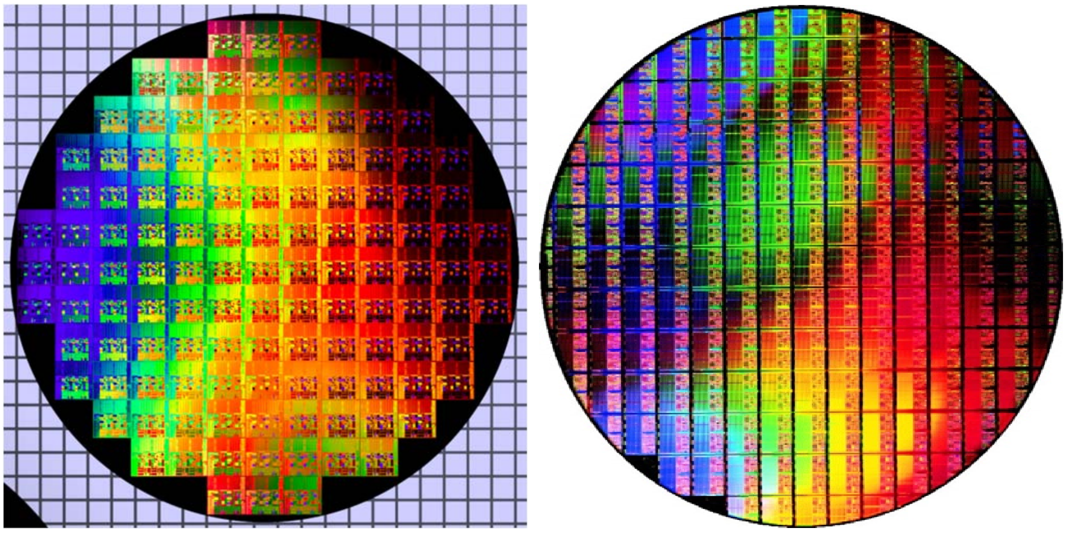
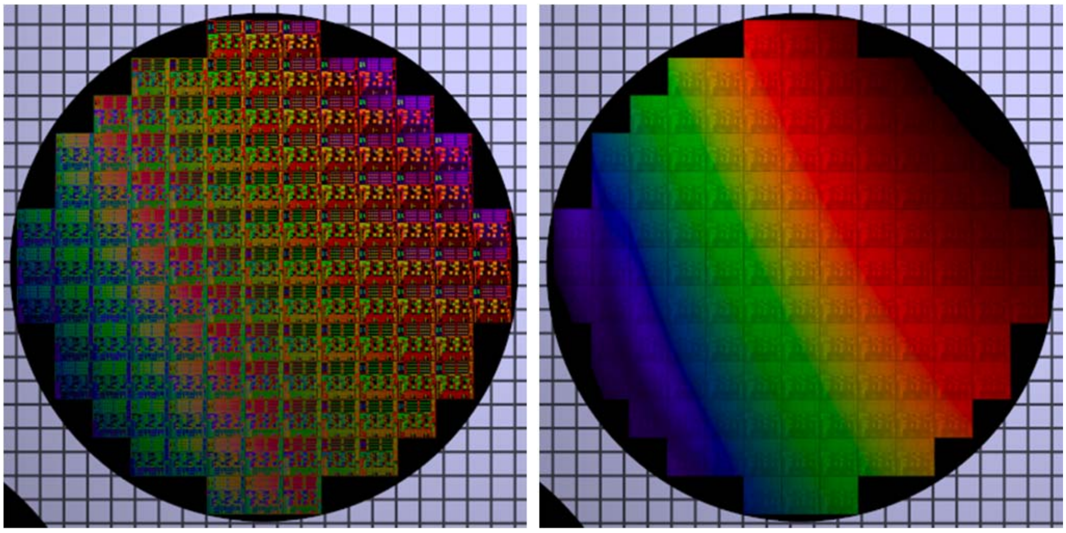


Figure 9. Comparison between rendering (left) and rotated photograph (right)

Challenges and Problems

During the rendering, we encountered and solved several problems, as discussed below.

The most difficult part is to extract the detailed structure of the die from the photograph. We know that the spacing between wires (notated as d in our report) is around 1 μm in common circuits, but it does have some variance. First we randomized d between 800 nm and 1200 nm, and got an image like Figure 10 (a). The colors were just too messy, and looked neither good nor similar to the photograph. We thought the reason was that the range of d was too large, so the colors in different areas of the dies hada different distributions, and they mixed up to get a disordered appearance.



(a) (b)

Figure 10. Some not-so-good-looking images

Then we narrowed down the range, to 1000 +/- 50 nm, as Figure 10 (b). A new problem came out, which was that it lacked the clear textures. Because in fact different blocks should have different parameters, too narrow range of d will eliminate this variance, and smooth the appearance of different blocks. Thus, we came to the final solution, which is to cluster the blocks into several groups, and use different means and variances for different groups. The largest block group will provide the background color patterns, and the other smaller groups can add spots or texture on it, as in our final rendering.

At last, a performance problem is that at first we changed the spectrum representation used in pbrt from RGB to sampled spectrum globally. That made the rendering slow down a lot, and was also very annoying to get rid of bugs. Later we found that sampled spectrum is only needed inside the BRDF calculation of the surface. Before we return to the global scope from the BRDF function, we can convert sampled spectrum back to RGB space, so the rest of the world will use RGB neatly, and run quickly.

Conclusion

We have successfully rendered the silicon wafer surface with rainbow colors shown on. The main physical reasons behind that are the interference and diffraction within or between the parallel metal wires on the top of the dies in the wafer. We study and model the structure of the surface. Then we analyze various physical effects that may affect the final appearance, and use BRDF to model their impacts. The final rendering looks very similar to the photograph, demonstrating the effectiveness of our method.

Teamwork

We worked together as a team to tune the final rendering. Mingyu was responsible for deriving the equations of diffraction and interference from physics principle, implementing them in pbrt, and also helping preparing the final scene. Jing put all BRDF together to make the IC material class and built the pbrt model of a single chip.

References

[1] C.-H. Jan et al, “RF CMOS technology scaling in High-k/metal gate era for RF SoC (system-on-chip) applications,” Electron Devices Meeting (IEDM), 2010 IEEE International, vol., no., pp.27.2.1,27.2.4, 6-8 Dec. 2010.

[2] Kevin Knapp, “Proper Planning Assures SoC Power Integrity”, Chip Design Magazine, December 2006/January 2007 issue.

[3] Yinlong Sun, F. David Fracchia, Mark S. Drew, and Thomas W. Calvert, “Rendering Iridescent Colors of Optical Disks”, In Proceedings of the Eurographics Workshop on Rendering Techniques 2000, Bernard Peroche and Holly E. Rushmeier (Eds.). Springer-Verlag, London, UK, UK, 341-352.